PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference M04-F-188CT1	**FOR FURTHER ACTION**	See Form PCT/IPEA/416
International application No. PCT/JP2004/016082	International filing date *(day/month/year)* 22.10.2004	Priority date *(day/month/year)* 26.12.2003

International Patent Classification (IPC) or national classification and IPC
INV. G11C11/56 G11C11/34 H01L45/00

Applicant
MATSUSHITA ELECTRIC INDUSTRIAL CO. ,LTD. ET AL.

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 14 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *sent to the applicant and to the International Bureau)* a total of 7 sheets, as follows:
      ☐ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in celectronic form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☒	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☒	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
18.10.2005	30.03.2006

Name and mailing address of the international preliminary examining authority:

European Patent Office - P.B. 5818 Patentlaan 2
NL-2280 HV Rijswijk - Pays Bas
Tel. +31 70 340 - 2040 Tx: 31 651 epo nl
Fax: +31 70 340 - 3016

Authorized officer

Colling, P

Telephone No. +31 70 340-4429

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/JP2004/016082

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This report is based on translations from the original language into the following language , which is the language of a translation furnished for the purposes of:
   - ☐ international search (under Rules 12.3 and 23.1(b))
   - ☐ publication of the international application (under Rule 12.4)
   - ☐ international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

Description, Pages

1-55	as originally filed

Claims, Numbers

1-9, 11-26, 28-31, 33-36, 38	as originally filed
10, 27, 32, 37, 39	received on 20.10.2005 with letter of 18.10.2005

Drawings, Sheets

1/30-30/30	as originally filed

☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. ☐ The amendments have resulted in the cancellation of:
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

* *If item 4 applies, some or all of these sheets may be marked "superseded."*

Box No. IV Lack of unity of invention

1. ☒ In response to the invitation to restrict or pay additional fees, the applicant has:
   - ☒ restricted the claims.
   - ☒ paid additional fees.
   - ☐ paid additional fees under protest.
   - ☐ neither restricted nor paid additional fees.

2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose, according to Rule 68.1, not to invite the applicant to restrict or pay additional fees.

3. This Authority considers that the requirement of unity of invention in accordance with Rules 13.1, 13.2 and 13.3 is

   ☐ complied with.

   ☒ not complied with for the following reasons:

   see separate sheet

4. Consequently, this report has been established in respect of the following parts of the international application:

   ☐ all parts.

   ☒ the parts relating to claims Nos. 1-11,21-39 .

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-11,21-38
	No:	Claims	39
Inventive step (IS)	Yes:	Claims	4,23,25,29,31,36
	No:	Claims	1-3,5-11,21,22,24,26-28,30,32-35,37-39
Industrial applicability (IA)	Yes:	Claims	1-11,21-39
	No:	Claims	

2. Citations and explanations (Rule 70.7):

   see separate sheet

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/JP2004/016082

Box No. VI Certain documents cited

1. Certain published documents (Rule 70.10)

   and / or

2. Non-written disclosures (Rule 70.9)

   see separate sheet

Re Item IV.

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1) claims 1-11,32-39: Multibit memory device;

2) claims 12-20: Memory device structure; and

3) claims 21-31: Memory circuit with fewer read/write errors

The International Searching Authority considers that the present application contains 3 inventions. This observation is based on the following reasoning:

Reference is made to the following document D1:

D1: ZHUANG W W ET AL: "Novel colossal magnetoresistive thin film nonvolatile resistance random access memory (RRAM)" INTERNATIONAL ELECTRON DEVICES MEETING 2002. IEDM. TECHNICAL DIGEST. SAN FRANCISCO, CA, DEC. 8 - 11, 2002, NEW YORK, NY : IEEE, US, 8 December 2002 (2002-12-08), pages 193-196, XP010626021 ISBN: 0-7803-7462-2.

Document D1 discloses (see memory array, figure 13, page 195, right hand column; the references in parentheses applying to this document) a memory device (a memory array) comprising a first variable resistor (first RRAM cell) connected between a first terminal (wordline GND) and a third terminal (bitline) having a resistance which changes in accordance with a polarity of a pulse voltage between the first terminal and the third terminal; and a second variable resistor (second RRAM cell) connected between the third terminal (same bitline) and a second terminal (wordline 0V) having a resistance which changes in a direction opposite to a direction of change of the first variable resistor in accordance with a polarity of a pulse voltage between the third terminal and the second terminal.

Hence all features of independent apparatus claim 1 are known from D1 and said claim

thus lacks novelty.

Dependent claim 2 and independent claim 12 share the following features:
a memory device comprising a (first) resistor having a resistance which changes in accordance with a polarity of a pulse voltage applied thereto.
These features are however known from prior art document D1 (see page 193, left-hand column, paragraph 2).
The special technical feature STF in the sense of Rule 13(2) PCT of claim 2 is thus constituted by:
the resistance value of the first variable resistor and the resistance value of the second variable resistor change in accordance with a first potential applied to two of the first terminal, second terminal and the third terminal and a second potential different from the first potential applied to the other terminal of the first terminal, the second terminal and the third terminal.
The problem to be solved by this feature could be said to be the provision of a multibit memory device (see description page 2, lines 10-25 of the present application).

Similarly independent claims 12 and 21 share the following features:
a memory device comprising a plurality of memory cells, each memory cell comprising a transistor connected to a variable resistor (layer) whose resistance value changes in response to a pulse voltage applied thereto.
These features are however also known from prior art document D1 (see figure 4)
The special technical feature STF in the sense of Rule 13(2) PCT of claim 12 is thus constituted by: an insulating layer formed over said transistor, said variable resistor film formed over the insulating layer.
The problem to be solved by this feature could be said to be the provision of a highly integrated memory cell with an increased degree of miniaturization
(see description page 3, lines 1-20 of the present application).

Similarly independent claim 21 and dependent claim 2 share the following features:
a memory device comprising a variable resistor connected between a first and a second terminal whose resistance value changes in response to a pulse voltage applied between said terminals.

These features are however also known from prior art document D1 (see page 193, left-hand column, paragraph 2).
The special technical feature STF in the sense of Rule 13(2) PCT of independent claim 21 is thus constituted by:
a first memory block connected between a first node and a second node; a first block selecting transistor connected in series with the first memory block between the first node and the second node; and a second memory block connected between an interconnect node and a third node, the interconnect node connecting the first memory block and the first block-selecting transistor to each other, wherein each of the first and second memory blocks includes a plurality of memory cells connected in series, and each of the plurality of memory cells including a transistor coupled in parallel with the variable resistor between the first and second terminal.
The problem to be solved by this feature could be said to be the provision of a memory circuit with fewer errors in recording and reproduction
(see description page 3, line 21 - page 4, line 25 of the present application).

The above analysis shows that there are no special technical features in the claimed 3 inventions, which are common. These features are not corresponding either, because they solve different, non related problems. Since common or corresponding STF's between the different inventions are missing, a technical relationship involving those features cannot be present
and the different inventions are thus not linked by a single general inventive concept.

Hence the present application does not meet the requirements of Unity of invention as defined in Rule 13(1) PCT.

Re Item V.

FIRST INVENTION: CLAIMS 1-11, 32-39

1. The following further document is referred to in this communication:

D2 : US 2003/038301 A1 (MOORE JOHN) 27 February 2003 (2003-02-27); and

2. The application does not meet the requirements of Article 6 PCT because:

2.1 The subject-matter of dependent claim 34 is redundant because, as far as it can be understood, said subject-matter is already included in parent claim 32.

2.2 The expression "a second potential" in claim 7 is unclear because a first potential has not been defined in claim 7 itself or its parent claim.

2.2 The expression "the first polarity" in claim 10 is undefined.

3. INDEPENDENT APPARATUS CLAIM 39 (amended)

The subject-matter of claim 39 is not new in the sense of Article 33(2) PCT and therefore does not meet the criteria of Article 33(1) PCT:

Document D2 discloses (see paragraphs [0021] - [0027] and figure 7; the references in parentheses applying to this document) a memory cell (dual cell common electrode programmable metallization (PCRAM) memory cell) suitable for storing at least one bit of data, comprising:

first variable resistance means (118) suitable for changing resistance in accordance with a polarity of a pulse voltage between a first terminal (source/drain of transistor 118_{AT}) and a third terminal (common anode 110); and

second variable resistance means (120) suitable for changing resistance in a direction opposite to a direction of change of the first variable resistance means in accordance with a polarity of a pulse voltage between the third terminal (110) and a second terminal (source/drain of transistor 120_{AT})
(for PCRAM cells, an increase or decrease of the memory cell resistance value depends on the polarity of the applied voltage to the two electrode terminals (anode, cathode) of the cell).

Thus all features of independent apparatus claim 39 are already known from D2 and said claim thus lacks novelty (Article 33(2) PCT).

4. INDEPENDENT APPARATUS CLAIM 1

The subject-matter of claim 1 does not meet the criteria of Article 33(1) PCT, because it

does not involve an inventive step in the sense of Article 33(3) PCT:

Document D2, which is considered to represent the closest prior art document, discloses (see paragraphs [0021] - [0027] and figure 7; the references in parentheses applying to this document) a memory device (dual cell common electrode programmable metallization (PCRAM) memory device), comprising:

a first variable resistor connected (118) between a first terminal (source/drain of transistor 118_{AT}) and a third terminal (common anode 110) having a resistance which changes in accordance with a polarity of a pulse voltage between the first terminal and the third terminal; and

a second variable resistor (120) connected between the third terminal (110) and a second terminal (source/drain of transistor 120_{AT}) having a resistance which changes in accordance with a polarity of a pulse voltage between the third terminal and the second terminal (for programmable metallization cells, an increase or decrease of the memory cell resistance value depends on the polarity of the applied voltage to the two electrode terminals (anode, cathode) of the cell).

The subject-matter of claim 1 therefore differs from this known from D2 only in that **the second variable resistor changes resistance in a direction opposite to a direction of change of the first variable resistor**

This selection of a resistance change direction out of two possible directions can only be regarded as inventive, if it presents unexpected effects or properties in relation to the other direction. However, no such effects or properties are indicated in the application, both devices i.e. the memory device of the present application and the memory device of D2, being multibit memory devices.

Hence the subject-matter of claim 1 cannot be considered as inventive.

5. INDEPENDENT METHOD CLAIMS 32 and 37 (amended)

The present application does not meet the criteria of Article 33(1) PCT, because the subject matter of independent method claims 32 and 37 does not involve an inventive step

in the sense of Article 33(3)PCT:

Independent method claims 32 and 37 claim a three terminal variable resistance memory cell writing/resetting method and reading method respectively, whereby different potential combinations are applied to the terminals of said memory cell. These methods are however equally applicable to the three terminal memory cell described in D2, figure 7 with the same result and the proposed methods in independent claims 32 and 37 thus cannot be considered as inventive (Article 33(3) PCT).

6. DEPENDENT CLAIMS 2-3, 5-11, 33-35, 38

As far as it can be understood, dependent claims 2-3, 5-11, 33-35, and 38 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty and/or inventive step (Article 33(2) and (3) PCT).

7. DEPENDENT CLAIMS 4 and 36

Presently it appears that the combination of the features of dependent claims 4 and the combination of the features of dependent claim 36 are neither known from, nor rendered obvious by, the available prior art. The reasons are that none of the cited prior art documents discloses nor suggests a memory cell comprising first and second variable resistance means arranged and biased as described in claims 4 or 36 thereby allowing multibit data storage.

THIRD INVENTION: CLAIMS 21-31

1. The following further documents are referred to in this communication:

D4: WO-A2-02 19337 (MOTOROLA INC.) 07 MARCH 2002 (2002-03-07);
D5: US-B1-6 226 197 (NAOKI NISHIMURA) 01 MAY 2001 (2001-05-01);
D6: US-A-5 969990 (KENSHIRO ARASE) 19 OCTOBER 1999 (1999-10-19).

2. INDEPENDENT APPARATUS CLAIM 21

The subject-matter of claim 21 does not meet the criteria of Article 33(1) PCT, because it

does not involve an inventive step in the sense of Article 33(3) PCT.

Document D4, which is considered to represent the closest prior art document, discloses (see page 7, line 26 - page 9, line 14 and figure 3; the references in parentheses applying to this document)

a memory circuit (magnetic tunnel junction random access memory 15) comprising:

a first memory block (16) connected between a first node (ground connection of block 16) and a second node (19);

a first block-selecting transistor (28) connected in series with the first memory block between the first node and the second node; and

a second memory block (17) connected between the second node (19) and a third node (ground connection of block 17);

wherein each of the first and second memory blocks includes a plurality of memory cells (18) connected in series, and

each of the plurality of memory cells includes

a variable resistor (magnetic tunnel junction 26) connected between a first terminal and a second terminal and whose resistance value changes in response to a pulse voltage applied between the first terminal and the second terminal, and

a transistor (27) connected in parallel with the variable resistor (magnetic tunnel junction 26) between the first terminal and the second terminal.

The subject-matter of claim 21 therefore differs from D4 in that said second memory block is connected between an interconnect node and a third node, the interconnect node connecting the first memory block and the first block-selecting transistor to each other (whereas in D4 a second block-selecting transistor is coupled between the second memory block and the second node (19)).

The problem to be solved by the present invention may therefore be regarded as the provision of a low disturb memory device using a reduced chip area.

A memory circuit wherein more than one memory block is connected through a block-selecting transistor is however known from D6 (see memory blocks NAND1a and NAND2a connected by block-selecting transistor TG1a to bitline MBLa in figure 2) and the skilled person, without the exercise of inventive skill, would thus consider to connect said second memory block at said interconnect node, in order to solve the problem posed.

Hence independent claim 21 cannot be considered to involve an inventive step.

Claim 21 does not explicitly claim that the first/second node is distinct from the third node and does not claim that different potentials are applied to the first/second node and the third node.

3. INDEPENDENT APPARATUS CLAIM 27 (amended)

The subject-matter of claim 27 does not meet the criteria of Article 33(1) PCT, because it does not involve an inventive step in the sense of Article 33(3) PCT.

Document D4, which is considered to represent the closest prior art document, discloses (see page 7, line 26 - page 9, line 14 and figure 3; the references in parentheses applying to this document)

a memory circuit **array having more than one column** (magnetic tunnel junction random access memory 15) comprising:

a first memory block (16) connected between a node receiving a fixed power supply (ground connection of block 16) and a first bit line (19);

a first block-selecting transistor (28) connected in series with the first memory block between the first bit line and the node;

a second memory block (16' in further column) connected between the node receiving the fixed power supply (ground connection of block 16') and a second bit line (19' in further column) different from the first bit line (19);

a second block-selecting transistor (28' in further column) connected in series with the second memory block between the second bit line and the node,

wherein each of the first and second memory blocks includes a plurality of memory cells (18) connected in series, and

each of the plurality of memory cells includes

a variable resistor (magnetic tunnel junction 26) connected between a first terminal and a second terminal and whose resistance value changes in response to a pulse voltage applied between the first terminal and the second terminal, and

a transistor (27) connected in parallel with the variable resistor (magnetic tunnel junction 26) between the first terminal and the second terminal.

Thus the subject-matter of claim 27 differs from a memory array of D4 only in that said power supply is variable (whereas in D4 said power supply is constant i.e. ground).
This feature however has to be considered as merely one of several straightforward possibilities from which the skilled person would select, in accordance with circumstances, without the exercise of any inventive skill.

Hence independent claim 27 cannot be considered to involve an inventive step.

4. DEPENDENT CLAIMS 22, 24, 26, 28, 30

Dependent claims 22-24, 26 and 28-30 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty and/or inventive step (Article 33(2) and (3) PCT) (see documents cited in search report, especially D5, column 10, line 40 - column 11, line 18 and figures 15 and 16).

5. DEPENDENT CLAIMS 23, 25 and 29, 31

It presently appears that the subject-matter of dependent claims 23, 29 and dependent claims 25, 31 fulfills the requirements of Article 33(1) PCT, because none of the cited prior art documents discloses nor suggests writing methods or reading methods respectively for a memory circuit wherein coordinated voltages are applied between complementary memory blocks.

6. Some of the features in dependent apparatus claims 22-25 and 28-31 relate to a method for reading and a method for writing a memory device rather than clearly defining the memory in terms of its technical features. The intended limitations are therefore not clear from these claims, contrary to the requirements of Article 6 PCT.

Re Item VI

Certain documents cited

Certain published documents

Application No Patent No	Publication date *(day/month/year)*	Filing date *(day/month/year)*	Priority date *(valid claim)* *(day/month/year)*
EP 1 426 966 A2	09.06.2004	04.12.2003	05.12.2002
EP 1 455 363 A1	08.09.2004	03.03.2004	06.03.2003

AMENDMENT

To : Examiner of the Patent Office

1. Identification of the International Application
PCT／JP2004／016082

2. Applicant
Name : MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
Address : 1006, Oaza Kadoma, Kadoma-shi, Osaka 5718501, JAPAN
Country of nationality : JAPAN
Country of residence : JAPAN

3. Agent
Name : (7793) Patent Attorney, MAEDA Hiroshi
Address : Osaka-Marubeni Bldg., 5-7, Hommachi 2-chome, Chuo-ku
Osaka-shi, Osaka, 5410053 Japan

4. Item to be Amended
Claims

5. Subject Matter of Correction
Claims 10, 27, 32, 37 and 39 should be amended as per the attached sheets.
Claim 10 is amended to define the first and second pulse voltages.
Claim 27 is amended to have the claim more distinct from Figure 3 in D4.
Claim 32 is amended to have the claim more distinct from D2.
Claim 37 is amended to have the claim more distinct from D2.
Claim 39 is amended to be more descriptive of the relation between the first, second and third terminals and the first and second variable resistance means.

6. List of Attached Documents
Pages 58, 62-1, 62-2, 63, 64-1, 64-2 and 65 of the Claims

10. (amended) The memory device of claim 1, wherein at a first time a first pulse voltage of the first polarity is applied to the first terminal and the third terminal and a second pulse voltage of polarity opposite to the first polarity is applied to the second terminal, and at a second time the second pulse voltage is applied to the third terminal and the second terminal and the first pulse voltage is applied to the first terminal.

11. The memory device of claim 1, wherein a voltage at the third terminal is output with a first potential applied to the first terminal and a second potential applied to the second terminal.

12. A memory device whose resistance value changes in accordance with a pulse voltage applied thereto, the device comprising:

a plurality of memory cells, each memory cell comprising:

a transistor formed on a semiconductor substrate and having a source, a drain and a gate;

an insulating layer formed over the transistor;

a variable resistance layer formed over the insulating layer; and

two electrodes formed on the variable resistance layer,

wherein at least one of the drain and the source of the transistor are electrically connected to the two electrodes.

13. The memory device according to claim 12, wherein each memory cell further comprises:

a conductive layer formed on the insulating layer; and

a contact plug electrically connecting the at least one of the drain and the

27. (amended) A memory circuit, comprising:

a first memory block connected between a node receiving a variable power supply and a first bit line;

a first block-selecting transistor connected in series with the first memory block between the first bit line and the node;

a second memory block connected between the node receiving the variable power supply and a second bit line different from the first bit line; and

a second block-selecting transistor connected in series with the second memory block between the second bit line and the node,

wherein each of the first and second memory blocks includes a plurality of memory cells connected in series, and

each of the plurality of memory cells includes

a variable resistor connected between a first terminal and a second terminal and whose resistance value changes in response to a pulse voltage applied between the first terminal and the second terminal, and

a transistor connected in parallel with the variable resistor between the first terminal and the second terminal.

28. The memory circuit of claim 27, wherein during writing of data,

the first block-selecting transistor and the second block-selecting transistor are turned ON,

a transistor in first a memory cell of the plurality of memory cells in the first memory block is turned OFF and a transistor in each memory cell other than the first memory cell of the plurality of memory cells in the first memory block is turned ON, and

a transistor in a second memory cell of the plurality of memory cells in the second

memory block is turned OFF and a transistor in each memory cell other than the second memory cell of the plurality of memory cells in the second memory block is turned ON.

29. The memory circuit of claim 28, wherein during writing of data, a pulse voltage for increasing the resistance value of a variable resistor included in the first memory cell is applied between the first node and the second node, and a pulse voltage for reducing the resistance value of a variable resistor included in the second memory cell is applied between the second node and the third node.

30. The memory circuit of claim 27, wherein during reading of data,

the first block-selecting transistor and the second block-selecting transistor are turned ON,

a transistor in a first memory cell of the plurality of memory cells in the first memory circuit is turned OFF and a transistor included in each memory cell other than the first memory cell of the plurality of memory cells in the first memory block is turned ON, and

a transistor in a second memory cell of the plurality of memory cells in the second memory circuit is turned OFF and a transistor in each memory cell of the plurality of memory cells other than the second memory cell is turned ON.

31. The memory circuit of claim 30, wherein during reading of data, a voltage at the second node is detected with a given voltage applied between the first node and the third node.

32. (amended) A method for writing of data in a variable resistance memory cell having at least three terminals and for resetting the variable resistance memory cell, comprising the steps of:

applying a first potential to two terminals of the at least three terminals of the variable resistance memory cell;

applying a second potential to a terminal other than the two terminals of the variable resistance memory cell;

changing a resistance value of a first variable resistance device of the variable resistance memory cell; and

changing a resistance value of a second variable resistance device of the variable resistance memory cell in a direction opposite to that of the first variable resistance memory device.

33. The method of claim 32, wherein during data writing, the second potential has a first polarity and during a resetting operation, the second potential has a second polarity opposite of the first polarity.

34. The method of claim 32, further comprising the steps of:

changing a resistance value of a first variable resistance device of the variable resistance memory cell;

changing a resistance value of a second variable resistance device of the variable resistance memory cell in a direction opposite to that of the first variable resistance memory device.

35. The method of claim 32, wherein

the step of applying the first potential comprises applying a first pulse of the first potential at a first time, and

the step of applying the second potential comprises applying a second pulse of the

second potential at the first time having a second polarity opposite of a first polarity of the first pulse.

36. The method of claim 35, further comprising the steps of:

applying a third potential of the second polarity to two terminals of the at

least three terminals of the variable resistance memory cell at a second time; and

applying a fourth potential of the first polarity to a terminal other than the two terminals of the variable resistance memory cell at the second time.

37. (amended) A method for reading of data in a variable resistance memory cell having at least three terminals, comprising the steps of:

providing the variable resistance memory cell having a common access transistor connected in series to an output node and a first variable resistance device and a second variable resistance device connected in parallel to the output node;

applying a ground voltage to a terminal of the first variable resistance device;

applying a reproducing voltage that is lower than a recording voltage to a terminal of the second variable resistance device;

outputting a voltage from the output terminal.

38. The method for reading of data according to claim 37, wherein the voltage output has multiple values corresponding to a number of voltage pulses applied in a recording operation.

39. (amended) A memory cell for storing at least one bit of data, comprising:

first variable resistance means for changing resistance in accordance with a polarity of a pulse voltage between a first terminal and a third terminal; and

second variable resistance means for changing resistance in a direction opposite to a direction of change of the first variable resistance means in accordance with a polarity of a pulse voltage between the third terminal and a second terminal.